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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/929,737	08/13/2001	Andreas Weber	15436.253.31	9021

7590 08/24/2005

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EXAMINER	
SINGH, DALZID E	
ART UNIT	**PAPER NUMBER**
2633	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/929,737	WEBER, ANDREAS	
	Examiner	Art Unit	
	Dalzid Singh	2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *34-41* is/are allowed.

6)☒ Claim(s) *1-3,6,9-16,19-25 and 27-33* is/are rejected.

7)☒ Claim(s) *4,5,7,8,17,18 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 32 and 33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 32 recites the limitation "the bias current" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3, 6, 9, 10, 13-16, 19, 20, 23-25 and 27-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Aronson et al (US Pub No. 2002/0149821).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome

either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, Aronson et al disclose an optoelectronic transceiver, as shown in Fig. 2 comprising:

a data transmit line coupled to an optical source (103);

a data receive line coupled to an optical detector (102);

a serial communication bus (15 and 16) distinct from the data transmit line and data receive line (see paragraph [0028], serial clock (SCL) and serial data (SDA) create serial communication bus);

a microprocessor (102) coupled to the serial communication bus, the microprocessor corresponding to a serial address (see paragraph [0014], Aronson et al disclose that the transceiver (GBIC) stores serial ID that can be read out via serial interface consisting of clock and data line or serial communication bus; the serial ID can be considered as address of the IC controller or microprocessor); and,

an optical driver (105) coupled to the optical source, the microprocessor providing a control signal for adjusting a swing amplitude of the optical driver in accordance with one or more commands received by the microprocessor via the serial communication bus (see paragraphs [0028-0029] and [0032-0033]; as shown Fig. 2, the controller is coupled to the communication bus (15 and 16) and to the laser driver (105)).

Regarding claim 2, Aronson et al disclose the optical source is supplied with a bias current, the microprocessor providing a control signal for adjusting the bias current of the optical source in accordance with the one or more commands received by the microprocessor via the serial communication bus (see paragraphs [0028-0029] and [0032-0033]; as shown Fig. 2, the controller is coupled to the communication bus (15 and 16) and to the laser driver (105)).

Regarding claims 3, 6 and 16, Aronson et al disclose the optical detector has an electrical bandwidth, the microprocessor providing a control signal for adjusting the electrical bandwidth of the optical detector in accordance with one or more commands received by the microprocessor via the serial communication bus (see paragraph [0045]; the rate selection signal is the command received by the controller to adjust the bandwidth).

Regarding claims 9, 19 and 27, Aronson et al disclose that the serial communication bus is a two-wire bus (see paragraph [0028]).

Regarding claims 10, 20 and 28, Aronson et al disclose that the control signal is an output voltage from the microprocessor (see paragraph [0032], the controller has multiplicity of D/A converters which may be implemented using voltage sources, therefore output voltage from the controller).

Regarding claims 13 and 23, the optoelectronic transceiver of claim 1, wherein the optical source is a laser diode (see paragraph [0013]).

Regarding claims 14 and 24, Aronson et al disclose that the optical driver is an integrated circuit (see paragraph [0026]).

Regarding claim 15, Aronson et al disclose an optoelectronic transceiver, as shown in Fig. 2 comprising:

a data transmit line coupled to an optical source (103);

a data receive line coupled to an optical detector (102);

a serial communication bus (15 and 16) distinct from the data transmit line and data receive line (see paragraph [0028], serial clock (SCL) and serial data (SDA) create serial communication bus);

a microprocessor (102) coupled to the serial communication bus, the microprocessor corresponding to a serial address (see paragraph [0014], Aronson et al disclose that the transceiver (GBIC) stores serial ID that can be read out via serial interface consisting of clock and data line or serial communication bus; the serial ID can be considered as address of the IC controller or microprocessor); and,

the optical source supplied with bias current, the microprocessor providing a control signal for adjusting the bias current of the optical source in accordance with one or more commands received by the microprocessor via the serial communication bus (see paragraphs [0032-0033]; D/A converter is used to directly control the laser bias current).

Regarding claim 25, Aronson et al disclose an optoelectronic transceiver, as shown in Fig. 2 comprising:

a data transmit line coupled to an optical source (103);

a data receive line coupled to an optical detector (102);

a serial communication bus (15 and 16) distinct from the data transmit line and data receive line (see paragraph [0028], serial clock (SCL) and serial data (SDA) create serial communication bus);

a microprocessor (102) coupled to the serial communication bus, the microprocessor corresponding to a serial address (see paragraph [0014], Aronson et al disclose that the transceiver (GBIC) stores serial ID that can be read out via serial interface consisting of clock and data line or serial communication bus; the serial ID can be considered as address of the IC controller or microprocessor); and,

the optical detector has an electrical bandwidth, the microprocessor providing a control signal for adjusting the electrical bandwidth of the optical detector in accordance with one or more commands received by the microprocessor via the serial communication bus (see paragraph [0045]; the rate selection signal is the command received by the controller to adjust the bandwidth).

Regarding claim 29, Aronson et al disclose the controller has multiplicity of D/A converter, which control laser bias current (see paragraph [0032]), therefore the D/A is a resistive network.

Regarding claim 30, Aronson et al disclose the controller has multiplicity of D/A converter, (see paragraph [0032]), the controller, which include the D/A converter, is an integrated circuit, therefore it is well known that integrated circuit is comprised of transistors.

Regarding claim 31, Aronson et al disclose optical detector, since the optical detector receives optical signal or lightwave, therefore it is inherent that the optical detector is a pin (photo intrinsic) diode.

Regarding claim 32 (as far as understood), Aronson et al disclose the controller has multiplicity of D/A converter, which control laser bias current (see paragraph [0032]), the controller, which include the D/A converter, is an integrated circuit, therefore it is well known that integrated circuit is comprised of transistors.

Regarding claim 33, as discussed above, the D/A converter receives control signal.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 9, 10, 11, 13-15, 19, 20, 21, 23, 24, 27 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sanchez (US Patent No. 6,629,638) in view of Gilliland et al (US Patent No. 6,554,492).

Regarding claim 1, Sanchez discloses an optoelectronic transceiver, as shown in Fig. 3, comprising:

a data transmit line (20) coupled to an optical source (274);

a data receive line coupled to an optical detector (3) (it would have been obvious that there exist a data received line so that the photodiode is able to received the signal);

an input/output interface (317) distinct from the data transmit line and data receive line (see col. 8, lines 30-33, Sanchez et al disclose input/output interface, it would have been obvious to provide such interface as serial communication bus);

a microprocessor (305) coupled to the serial communication bus; and,

an optical driver (350) coupled to the optical source, the microprocessor providing a control signal for adjusting the a swing amplitude of the optical driver in accordance with one or more commands received by the microprocessor via the serial communication bus (see col. 9, lines 66-67 to col. 10, lines 1-13; the adjustment of the driver provide variation on the amplitude level of the optical signal, therefore results in "swing amplitude"; in col. 8, lines 30-33, Sanchez et al disclose that the input/output interface received control signal, it would have been obvious to consider that such control signal is command signal).

Sanchez discloses processor as discussed above and differs from the claimed invention in that Sanchez does not disclose that the microprocessor corresponding to a serial address. However, it is well known to provide serial address to processor. Gilliland et al is cited to show such well known concept. In col. 5, lines 2-7, Gilliland et al disclose assigning address to module. Therefore, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to provide address

to the module such as microprocessor or processor. One of ordinary skill in the art would have been motivated to do such in order to identify a particular device.

Regarding claim 2, as shown in Fig. 3, Sanchez shows that the optical source (274) is supplied with a bias current (I_{DC}), the microprocessor providing a control signal (D_1) for adjusting the bias current of the optical source in accordance with the one or more commands received by the microprocessor via the serial communication bus (in col. 8, lines 30-33, Sanchez et al disclose that the input/output interface received control signal, therefore it would have been obvious to consider that such control signal is command signal).

Regarding claims 9, 19, 27 and 35, as discussed above Sanchez discloses input/output interface, which is considered as serial communication bus, and differ from the claimed invention in that Sanchez does not specifically disclose that the serial communication bus is a two-wire bus. However, in communication system it is well know to provide two-wire bus. Gilliland et al teach such well known concept. In col. 1, lines 48-51, Gilliland et al disclose two-wire bus. Therefore, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to provide two-wire bus as the input/output interface of Sanchez. One of ordinary skill in the art would have been motivated to do such in order provide easier access.

Regarding claims 10 and 20, as shown in Fig. 3, Sanchez shows that the control signal (D_1, D_2, D_3 and D_4) is an output voltage from the microprocessor (it would have been obvious that such signals comprise of voltage level).

Regarding claims 11 and 21, as shown in Fig. 3, Sanchez shows that the control signal is a voltage from a resistor network wherein the resistor network receives an output voltage from the microprocessor (the output from the microprocessor (305) is transmitted to DAC circuit which comprise of internal circuit components; it is well known that circuit component posses resistance; therefore the circuit element within DAC circuit form a resistive network).

Regarding claims 13 and 23, Sanchez discloses that the optical source is a laser diode (see col. 7, lines 51-52).

Regarding claims 14 and 24, the combination of Sanchez and Gilliland et al discloses optical driver (350) (see Fig. 3 of Sanchez) and differ from the claimed invention in that Sanchez does not specifically disclose that the driver is an integrated circuit. However, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to provide integrated driver. One of ordinary skill in the art would have been motivated to do such in order to provide energy efficient and cost saving system.

Regarding claim 15, Sanchez discloses an optoelectronic transceiver, as shown in Fig. 3, comprising:

a data transmit line (20) coupled to an optical source (274);

a data receive line coupled to an optical detector (3) (it would have been obvious that there exist a data received line so that the photodiode is able to received the signal);

an input/output interface (317) distinct from the data transmit line and data receive line (see col. 8, lines 30-33, Sanchez et al disclose input/output interface, it would have been obvious to provide such interface as serial communication bus);

a microprocessor (305) coupled to the serial communication bus; and,

the optical source supplied with a bias current, the microprocessor providing a control signal for adjusting the bias current of the optical source in accordance with one or more commands received by the microprocessor via the serial communication bus (see col. 9, lines 52-65; in col. 8, lines 30-33, Sanchez et al disclose that the input/output interface received control signal, therefore it would have been obvious to consider that such control signal is command signal).

Sanchez discloses processor as discussed above and differs from the claimed invention in that Sanchez does not disclose that the microprocessor corresponding to a serial address. However, it is well known to provide serial address to processor. Gilliland et al is cited to show such well known concept. In col. 5, lines 2-7, Gilliland et al disclose assigning address to module. Therefore, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to provide address to the module such as microprocessor or processor. One of ordinary skill in the art would have been motivated to do such in order to identify a particular device.

7. Claims 12, 22, 30 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sanchez (US Patent No. 6,629,638) in view of Gilliland et al (US Patent No. 6,554,492) and further in view of Banniza et al (US Patent No. 5,680,060).

Regarding claims 12, 22, 30 and 38, the combination of Sanchez and Gilliland et al discloses digital to analog converter (DAC) which comprises of resistor network and differ from the claimed invention in that the combination does not disclose that the resistor network includes a transistor. However, it is well known that resistor network such as the digital to analog converter comprise of transistor. Banniza et al is cited to show such well known concept. In col. 6, lines 16-25, Banniza et al disclose digital to analog converter comprising of transistor. Therefore, it would have been obvious that the resistor network such as the digital to analog converter of Sanchez comprised of transistor. The motivation of providing transistor for the resistor network to increase speed.

Allowable Subject Matter

8. Claims 34-41 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Claim 34 is allowable because the prior arts of record do not specifically teach of fairly suggest optoelectronic transceiver comprising:

a serial communication bus distinct from the data transmit line and data receive line;

a microprocessor coupled to the serial communication bus, the microprocessor corresponding to a serial address;

the optical detector has an electrical bandwidth, and

a plurality of filter components, the microprocessor providing control signals to the filter components for coupling to the optical source or the optical detector in accordance with one or more commands received by the microprocessor via the serial communication bus.

9. Claims 4, 5, 7, 8, 17, 18 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Byers (US Patent No. 5,781,320) is cited to show fiber access in telecommunication network.

Ames et al (US Patent No. 2003/0002108) is cited to show fiber optic transceiver.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dalzid Singh whose telephone number is (571) 272-3029. The examiner can normally be reached on Mon-Fri 9am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (571) 272--3022. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DS
August 16, 2005
David Singh